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ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, NOV / DEC 2024

ELECTRONICS AND COMMUNICATION ENGINEERING

V Semester

EC5077 &amp; REAL TIME EMBEDDED SYSTEMS

(Regulation2019)

Time:3hrs

Max.Marks: 100

CO1	Ability to design and develop ARM processor based systems.
CO2	Ability to comprehend and appreciate the significance and role of microcontrollers in embedded systems.
CO3	Ability to analyze and demonstrate program design and optimization and proper scheduling of the process.
CO4	Ability to apply the concept of process, multi processes and operating systems in embedded system design.
CO5	Ability to implement various communication protocols in distributed embedded computing platform.

**BL – Bloom's Taxonomy Levels**

(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

**PART- A(10x2=20Marks)**

(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
1	Compare the basic task of SWI and SWP instructions	2	1	L2
2	Write an ARM assembly code to implement the following loops: for (i = 0; i < 10; i++) for (j = 0; j < 10; j++) z[i] = a[i, j] * b[i]	2	1	L3
3	Differentiate burst mode and page mode operations.	2	2	L1
4	What is the average memory access time of a machine whose hit rate is 93%, with a cache access time of 5 ns and a main memory access time of 80 ns?	2	2	L2
5	For basic block given below, rewrite it in single-assignment form, and then draw the data flow graph for that form. w = a - b + c; x = w - d; y = x - 2; w = a + b - c; z = y + d; y = b * c;	2	6	L2
6	List out the technique which are used to optimize execution time of a program?	2	3	L1
7	The Periodic tasks are given below  Task   Period   Execution time P1      5 ms      2 ms P2      10 ms     3 ms P3      10 ms     3 ms P4      15 ms     6 ms  Compute the utilization of this set of tasks.	2	4	L5

8	How is a Real time operating system uniquely different than a general purpose OS?	2	4	L1
9	Mention the networks for distributed embedded systems.	2	5	L2
10	How would you highlight the use of exponential back off technique?	2	5	L1

**PART- B(5x 13=65Marks)**  
(Restrict to a maximum of 2 subdivisions)

Q.No.	Questions	Marks	CO	BL																		
11 (a)(i)	Examine in detail about the challenges in embedded computing system design and its characteristics and performance.	5	1	L2																		
(a)(ii)	Mention the requirements for designing a GPS moving map in embedded system design process and Write down the major operations and data flows with its block diagram and sketch the hardware and software architecture of a moving map.	8	1	L2																		
<b>OR</b>																						
11 (b)(i)	Design and write an program to implement accurate speed control of electric car using ARM processor. List the various system requirements with complete architecture using UML diagrams.	9	1	L2																		
(b)(ii)	Discuss about the three addressing modes of C55x in detail and differentiate between two types of subroutine slow and fast returns	4	1	L2																		
<b>OR</b>																						
12 (a)(i)	Describe in detail about the basic sources of CMOS power consumption and give the power-saving strategies used in CMOS CPUs. Mention the Power-saving modes of the StrongARM SA-1100 with the state machine.	6	2	L3																		
(a)(ii)	Determine the Huffman code and efficiency of code for the following message with their probabilities given	7	2	L3																		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>i</td></tr> <tr> <td>0.36</td><td>0.15</td><td>0.13</td><td>0.11</td><td>0.09</td><td>0.07</td><td>0.05</td><td>0.03</td><td>0.01</td></tr> </table>	a	b	c	d	e	f	g	h	i	0.36	0.15	0.13	0.11	0.09	0.07	0.05	0.03	0.01			
a	b	c	d	e	f	g	h	i														
0.36	0.15	0.13	0.11	0.09	0.07	0.05	0.03	0.01														
<b>OR</b>																						
12 (b)(i)	Draw a timing diagram that shows a complete DMA operation, including handing off the bus to the DMA controller, performing the DMA transfer, and returning bus control back to the CPU.	6	2	L3																		
(b)(ii)	Explain in detail about the internal organization of memory device, Random access memories and Read only memories with necessary timing diagram and examples.	7	2	L3																		
<b>OR</b>																						
13 (a)(i)	Illustrate with necessary diagrams about the program level performance analysis for the real time embedded systems.	7	3	L5																		
(a)(ii)	Show the contents of the assembler's symbol table at the end of code generation for each line of the program: ORG 200 p1 ADR r4, a LDR r0, [r4] ADR r4, e LDR r1, [r4] ADD r0, r0, r1 CMP r0, r1 BNE q1 p2 ADR r4,e	6	3	L5																		
<b>OR</b>																						
13 (b)(i)	Elaborate in detail about Program Validation and Testing strategies Methods by exercising programs in different ways.	7	3	L5																		



(b)(ii)	Design a fixed baud rate frequency-shift keyed modem with theory of operation, requirement, specification, system architecture and give its relevant diagrams.	6	3	L5
14 (a)(i)	Enumerate why an automobile engine requires multi rate control.	4	4	L4
(a)(ii)	With necessary illustrations and C-code explain about Earliest – Deadline – First algorithm for scheduling three process with hyper period 60 .	9	4	L4
<b>OR</b>				
14 (b)(i)	With neat sketches, explain in detail about how shared memory communication and message passing mechanisms are used for inter process communication.	6	4	L4
(b)(ii)	How would you use the ADPCM method to encode an unvarying (DC) signal with the coding alphabet whose values are in a relative range that spans both negative and positive values.	7	4	L4
15 (a)(i)	With a neat block diagram, explain briefly how the CPU cache causes problems for accelerators and also suggest a technique by which the problem could be overcome?	8	5	L3
(a)(ii)	With an example, explain how does single threaded or multithreaded control of an accelerator will affect the speedup factor?	5	5	L3
<b>OR</b>				
15 (b)	Outline the concepts of interconnect networks for distributed embedded computing I <sup>2</sup> C and CAN bus protocol with neat architecture and data format.	13	5	L3

**PART- C(1x 15=15Marks)**  
(Q.No.16 is compulsory)

Q.No.	Questions	Marks	CO	BL
16(i)	Consider a size of main memory with 128 KB and cache of size 16 KB with block size 256 bytes. Find the Number of bits in tag and Tag directory size. Represent the address space in direct mapping and 2-way set associative mapping.	7	2	5
16(ii)	Design and implement an embedded system for a smart agriculture system that monitors and controls irrigation, soil moisture, and temperature and also analyze energy and power consumption with program optimization strategies.	8	5	6

